Short Papers

Determination of Schottky Diode Sampling Mixer Frequency Response From Diode Conductance Waveforms

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Abstract— **Conversion loss variations at microwave frequencies for Schottky diode harmonic sampling mixers are predicted from a time and frequency domain analysis of diode conductance waveforms. A circuit model for the mixer is used to find a nonlinear integral-differential equation governing the sampling mixer's time domain behavior. An iterative solution is used to determine the diode conductance waveform, whose fourier transform is the frequency response of the sampler. Experimental verification is given for three different values of sampling capacitors and two different sampling chamber delays over a 2 to 40 GHz range.**

I. Introduction

Sampling mixers are widely used in microwave phase-locked synthesizers and instrumentation. The IF output port of a sampling mixer provides a frequency periodic translation of a microwave signal input to the RF port. A low-pass filter on the IF port passes only the output component generated by the product of the input microwave signal and the nearest sampling frequency harmonic. Relative amplitude and phase characteristics are preserved in the downconversion, allowing the utilization of phase-locking or digital frequency counting circuits [1], [2].

Conversion loss variations over the microwave frequency range have been determined based on the assumption that the sampling waveform is a rectangular pulse of width, τ, and repetition period, T [2], [3]. A sinc (τf) response is predicted from the idealization where f is the RF input signal frequency. The location of nulls in the frequency response is a function of the pulse width, usually set by the round trip delay time of the even mode in a coplanar waveguide chamber [1]. However, in many practical sampling mixer implementations, SRDs with finite transition times generate the leading edge, and sampling capacitors in the 0.2 to 2 pF range hold the signal for IF combining purposes. For a range of realizable SRD rise times, capacitor values, and round trip delays, the sampling waveforms differ significantly from the rectangular approximation.

In this paper, an analytical model is used to simulate the behavior of Schottky diode sampling mixer circuits. The nonlinear integral-differential equation developed from the model is analyzed to describe time domain behavior. Standard iterative techniques are employed to solve the nonlilnear time domain equation for the diode's conductive waveform. The sampling mixer frequency response is found from the Fourier transform of the diode conductive waveform. The xomputed frequency response is then compared to experimental conversion loss data over a 2 to 40 GHz range. The analysis shows that nulls predicted for long, round trip delay times using the rectangular pulse approximation are not necessarily present in the frequency response. Results are applicable to the design of sampling mixers that are insensitive to variations in SRD parameters and therefore are suitable for high volume manufacturing techniques.

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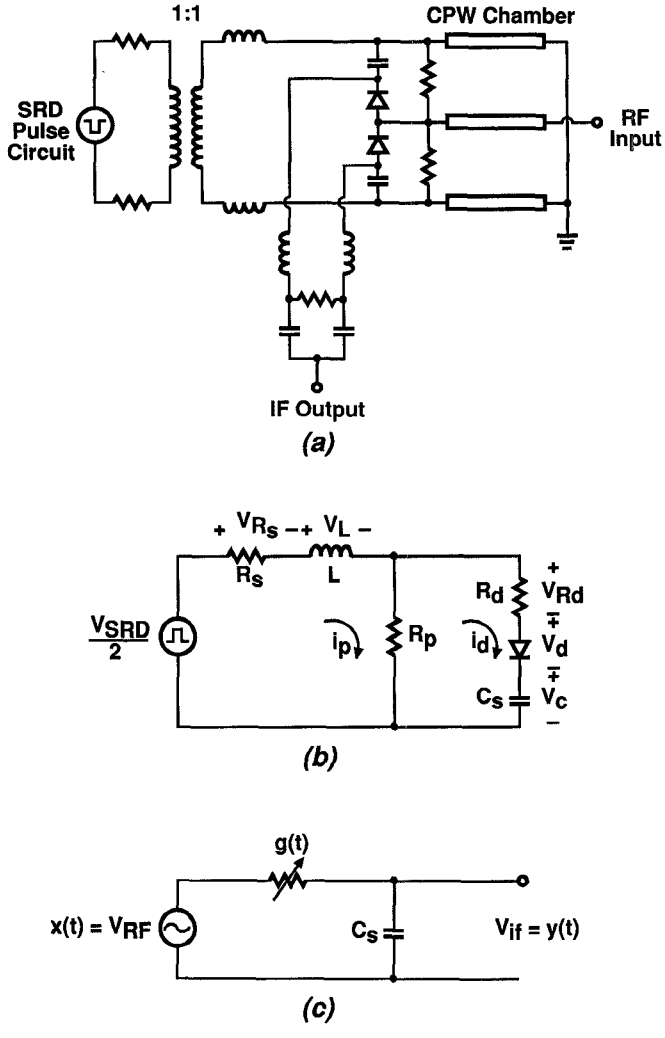

Fig. 1. (a) Sampling mixer schematic, (b) model for determining $g(t)$, and (c) model for determining $y(t)$.

II. Sampling Mixer Analysis

Fig. 1(a) is a schematic diagram of the hybrid sampling mixer. The RF input transmission line is coplanar-waveguide (CPW) and a transmission-line balun applies a balanced LO signal to the coplanar-strips (CPS). Round trip delay times are determined by the length of the CPW section [1]. A virtual ground for the LO pulse exists at the CPW center conductor, allowing the circuit to be bisected lengthwise for analysis, Fig. 1(b). The SRD-CPW pulsing circuit in Fig. 1(a) is replaced in Fig. 1(b) by a pulse source characterized by pulse width T_p, Thevinin impedance R_s, parasitic bond wire inductance L_s, and transition time T_{srd}. A series resistance R_d, and nonlinear current element

$$I_d = I_o\,(e^{qV_d/\eta kT} - 1) \tag{1}$$

models the Schottky diode [4]. Other parasitics such as the diode's junction capacitance are ignored, as is the IF combining circuit. By

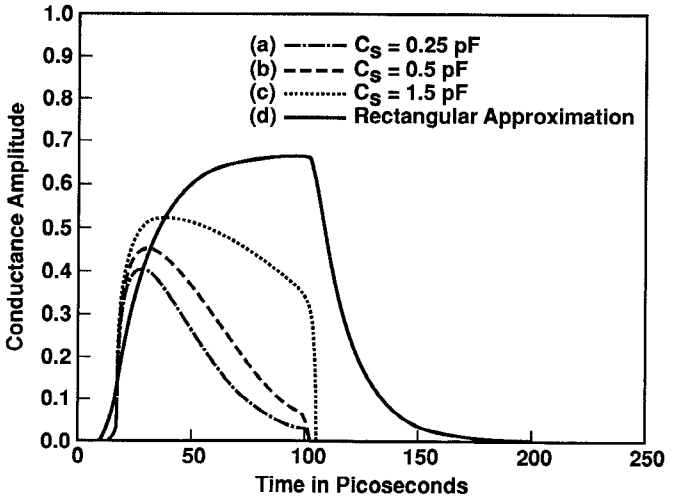

Fig. 2. Diode conductance waveforms computed from the model for (a) 0.25 pF, (b) 0.5 pF, and (c) 1.5 pF sampling capacitors, and (d) the ideal pulse approximation which is scaled version of V_{SRD}. All four plots used T_{SRD} = 35 ps, 90 ps CPW chamber delay, R_s = 25 Ohms, R_p = 100 Ohms, R_d = 1.5 Ohms, and L = 0.3 nH.

substituting (1) into the voltage loop equation

$$V_c + V_d + V_L + V_{Rs} + V_{Rd} - \frac{V_{\mathrm{SRD}}}{2} = 0 \tag{2}$$

the following nonlinear integral-differential equation that describes the time behavior of the diode voltage is found

$$\begin{aligned}&\frac{I_0}{C}\left(1+\frac{R_s}{R_p}\right)\int_o^t (e^{qV_d/\eta kT}-1)\,dt \\ &+ I_o\,(e^{qV_d/\eta kT}-1)\left[R_d + R_s + \frac{L}{R_pC} + \frac{R_s R_d}{R_p}\right] \\ &+ V_d\left[1+\frac{R_s}{R_p}\right] \\ &+ \frac{dV_d}{dt}\left[\frac{L}{R_p} + \frac{qLI_o}{\eta kT}\,e^{qV_d/\eta kT}\left(1+\frac{R_d}{R_p}\right)\right] \\ &- \frac{V_{\mathrm{SRD}}}{2} = 0\end{aligned} \tag{3}$$

A finite difference solution was implemented to determine V_d for an exponentially rising and decaying pulse function $V_{\mathrm{SRD}}/2$. A bisection search algorithm [5] was employed to obtain an iterative solution to the V_d time vector. Convergence accuracy was constrained to be better than 0.1 millivolt with a time resolution of 1 ps. Sampling diode current I_d is computed directly from V_d. The diode conductance is

$$g(t) = \frac{1}{1/(dI_d/dV_d) + R_d} \tag{4}$$

where the peak magnitude of the diode conductance is set by the current independent ohmic loss term R_d, and I_d is given by (1).

Computed diode conductance waveforms for three different values of sampling capacitors are plotted in Fig. 2(a)–(c) for a 35 ps 10%–90% SRD rise time and a CPW round trip delay of 90 ps. A comparison between C_s = 0.25, 0.5, and 1.5 pF shows that the average time duration of the conductance waveform is dependent on the sampling capacitor value for a given SRD pulsing circuit. When the SRD pulse forces the diode into conduction, the diode current charges the sampling capacitor. The sampling capacitor voltage decreases the diode current to a fraction of the peak value before the reflected SRD pulse returns. After the 90 ps round trip delay, the conductance pulse is abruptly terminated. The ideal pulse approximation, where only the SRD rise time and CPW chamber delay time is considered, is plotted in Fig. 2(d).

Fig. 1(c) describes the model for the RF sampling process. The sampling waveform, $s(t)$, that under-samples an input RF signal $x(t)$, is found from the diode conductance waveform. For a periodic sample pulse train,

$$s(t) = \left(\frac{A}{C}\sum_{n=-\infty}^{\infty}\delta(t-nT)\right) * g(t) \tag{5}$$

where $*$ denotes convolution, A is an arbitrary scaling constant, and T is the repetition rate of the sample pulse. The $1/C$ factor is included to account for the inverse relationship between sampling capacitance and sampled IF output voltage magnitude. In the frequency domain the sampling waveform spectrum is

$$S(f) = \frac{A}{TC}\left(\sum_{n=-\infty}^{\infty}\delta(f-n/T)\,G(n/T)\right) \tag{6}$$

IF output products $Y(f) = F(y(t))$ are readily found in the frequency domain as the convolution of the signal spectrum with the sampling waveform spectrum

$$Y(f) = X(f) * \frac{A}{TC}\left(\sum_{n=-\infty}^{\infty}\delta(f-n/T)\,G(n/T)\right) \tag{7}$$

Microwave applications often require only the lowest output frequency term in (7), which is isolated from higher frequency terms by a low-pass filter. The term in (7) that determines the frequency response of the sampler is the frequency spectrum of the sampling waveform evaluated at the impulse harmonic nearest to the input signal frequency. Assuming a cosinusoidal RF signal at a frequency f_o is input to the mixer, and N/T is the sample frequency harmonic nearest f_o, then after low-pass filtering (7) reduces to

$$\begin{aligned}Y_{\mathrm{LPF}}(f) = \frac{A}{2TC}\big(&\delta(f-f_o+N/T)\,G(-N/T) \\ &+ \delta(f+f_o-N/T)\,G(N/T)\big)\end{aligned} \tag{8}$$

Taking the magnitude, the frequency response of the low-pass filtered sampler is directly proportional to the spectrum magnitude of the sampling waveform, and inversely proportional to the sample period T. Thus the fourier transform of the conductance waveform will reveal the frequency response shape for a sampling mixer.

III. Results and Experimental Verification

A hybrid thin-film circuit that utilizes a GaAs sampling mixer MMIC was used to check the validity of the computer model. Fig. 3 shows the GaAs sampling chip in a coplanar waveguide mixer circuit that has 90 ps round trip chamber delay. The test was performed by sequentially installing three different GaAs chips, which are identical except for the sampling capacitance values, into the circuit and measuring conversion loss over a 2 to 40 GHz range. Sampling capacitor values were 0.25, 0.5, and 1.5 pF. Excitation to the SRD pulsing circuit was set to 1.5 GHz at 20 dBm throughout the experiment. The L-band sampling frequency was selected to insure that conversion efficiency for the 0.25 pF case would not degrade as a result of the capacitor's inability to hold charge over the full sample period. Variations in conversion loss due to the RF source and IF amplifier were held to within ±1 dB by making measurements at a discrete set of RF frequencies that maintained a 50 MHz IF output signal.

Fig. 4 summarizes the conversion efficiency vs. frequency measurements and compares them to computed frequency responses. Predicted conversion efficiencies are fast Fourier transforms of the

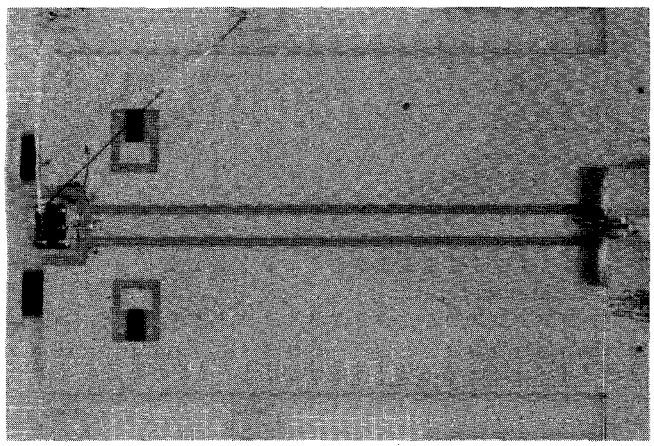

Fig. 3. Sampling mixer GaAs MMIC and hybrid circuit. RF at the right is launched into the CPW chamber from a microstrip line, a balanced SRD pulse on coplanar strips (CPS) is incident from the left, and the IF output is at the top of the circuit.

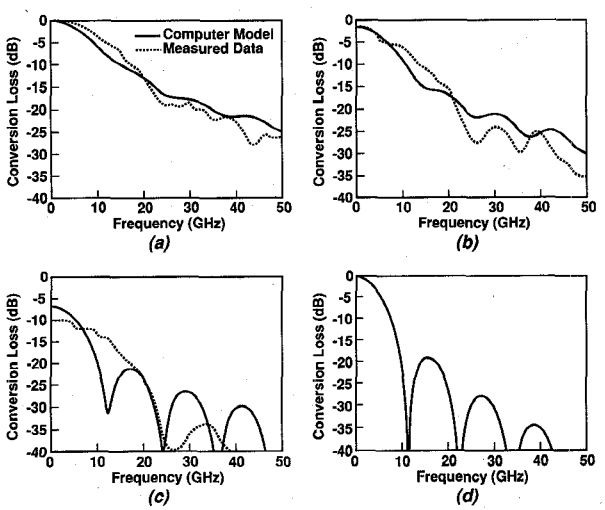

Fig. 4. Measured and predicted sampler frequency response for (a) 0.25 pF, (b) 0.5 pF, and (c) 1.5 pF sampling capacitors, and (d) the spectrum predicted from the ideal pulse approximation. Measured results are for F_{LO} = 1.5 GHz, and a discrete set of RF frequencies was used such that F_{IF} = 50 MHz. The predicted responses are FFTS of conductance waveforms from Fig. 2. Plots (a)–(c) have been normalized to the 0.25 pF case at low frequencies. T_{SRD} = 35 ps, 90 ps CPW chamber delay.

conductance waveforms shown in Fig. 2. The predicted and measured responses have been normalized to the lowest conversion loss for the three sampling capacitor values. Correlation is good given the simplicity of the computer model. As can be seen in parts (a)–(c) of Fig. 4, nulls in the response are minimal for the 0.25 pF case, but increase in depth with increasing sampling capacitor values. The observation is attributable to the long CPW chamber delay time. Fig. 4(d) presents the predicted frequency response using the ideal pulse approximation shown in Fig. 2(d). The results show that the conductance waveform model is an improvement on the ideal pulse approximation.

Shorter round trip delays, described in [6]–[8], truncate the natural response of the diode conductance waveform. A 35 ps round-trip chamber delay for the 0.25 pF sampler was formed by shorting out the CPW even mode ground planes with gold bond wires. The new computed diode conductance waveform for this configuration is shown in Fig. 5(a) and conversion loss measurements are compared to the computer model in Fig. 5(b).

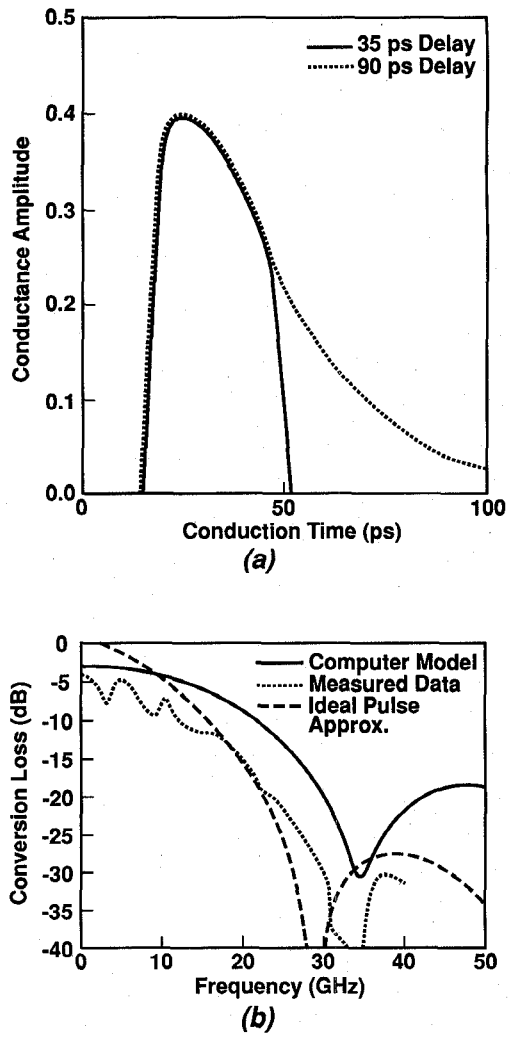

Fig. 5. (a) Diode conductance waveform computed from the model for 0.25 pF sampling capacitors and two different CPW chamber delays (35 ps and 90 ps). T_{SRD} = 35 ps, R_s = 25 Ohms, R_p = 100 Ohms, R_d = 1.5 Ohms, and L = 0.3 nH. (b) Measured and predicted frequency response for a sampler with 35 ps CPW chamber delay and 0.25 pF sampling capacitors. T_{SRD} = 35 ps, R_s = 25 Ohms, R_p = 100 Ohms, R_d = 1.5 Ohms, and L = 0.3 nH.

IV. Discussion

The analysis results presented in Fig. 4 predict that the sampler frequency response becomes more similar to a sinc (τf) response with increasing sampling capacitance or a shorter chamber delay. This is due to a more abrupt termination of the conductance waveform. For small sampling capacitance values, the conductance has decayed to a fraction of the peak value before the reflected pulse returns to truncate the waveform. The conductance magnitude is a greater percentage of the peak value when truncation occurs for the larger capacitance values, thus increasing the depth of the sinc (τf) nulls in the frequency response. The effect can be seen by comparing parts (a)–(c) of Fig. 2 and also Fig. 4. The model presented here shows good correlation with experimental data for the 0.25 and 0.5 pF cases, while there is a significant discrepancy in the depth of the first sin (τf) null for the 1.5 pF case. Tests were made on four separate sampling mixer circuits with 1.5 pF capacitors to verify the discrepancy, all units had less than 5 dB nulls at 10 GHz. The error for 1.5 pF is believed to be partially attributable to neglecting of the IF combining circuit in the computer model.

Based on this analysis, it is expected that some sampling mixer applications would benefit from the use of round trip delays that

TABLE I
SAMPLING MIXER SPECIFICATIONS

	Sampling Mixers	Specifications	
W-J Model No.	LO Frequency (GHz)	RF Frequency (GHz)	Conversion Loss (dB Max.)
6300–310	.200±.02	2–18	25
6300–340	1.000±.100	2–18	15
6300–370	1.000–1.500	2–18	22

are much longer than would seem appropriate according to the ideal pulse approximation. The 90 ps 0.25 pF circuit evaluated here has a monotonically decreasing output that is usable to 40 GHz (Fig. 4(a)). The same sampler modified for a 35 ps chamber delay exhibits lower conversion efficiency and a deep null at 34 GHz (Fig. 5(b)). Care must be exercised in selecting the sampling frequency of operation. For example, operating the 0.25 pF circuit at the 300 MHz sampling frequency used in [8] would be undesirable since the capacitor value is not suitable to hold the sampled signal over the duration of the sample period. VHF sampling rates require higher sampling capacitor values and faster SRD rise times to achieve Ka band operation.

Sensitivity to the pulse generator rise time for the 90 ps chamber delay sampler was investigated using four different SRD lots from three different manufacturers. The SRDs had 10%–90% transitions times in the 35 to 60 ps range. After the SRD matching network was adjusted, all four versions of the circuit were within the production performance specifications listed in Table I. In contrast, units that employ much shorter round-trip chamber delays often require a number of SRD lot evaluations before finding diodes with acceptable rise times.

V. CONCLUSION

A computer model has been developed to aid in the understanding of sampling mixer conversion loss variations at microwave frequencies. Conversion loss is predicted using the fourier transform of diode conductance waveforms. Experimental verification was given for three different values of sampling capacitors over a 2–40 GHz range. Results have been used to design a product line of integrated sampling mixers that are amenable to production manufacturing and insensitive to variations in SRD parameters.

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Parameter Extraction of Microwave Transistors using a Hybrid Gradient Descent and Tree Annealing Approach

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***Abstract*—Tree annealing is a robust optimization scheme which can be used to find the "valleys" of an error surface. The problem of entrapment in local minima is not a factor with this type of optimization, however, it is much slower than gradient-based techniques. The method presented here attempts to take advantage of the speed of gradient-based methods and of the efficient pseudo-random searching abilities of tree annealing. The result is a technique which behaves as a directed multi-start gradient method. All minima encountered during optimization are recorded, thus providing alternatives in case of a non-physical final solution. The technique is used in the extraction of a modified Materka-Kacprzak model of a GaAs MESFET.**

I. INTRODUCTION

Circuit designers rely on models of active devices to design and simulate active microwave circuits prior to fabrication. The ability to determine accurately the parameters of these models has been limited by the lack of a sufficiently accurate equivalent circuit and a tool that extracts consistently reliable model parameters from device measurements and model predictions. Gradient-descent algorithms are most commonly used but results are seldom satisfactory unless the initial estimate of parameter values is very good. Measurement error, coupled with the large number of elements of a physically-based equivalent circuit, leads to an error function having many minima. If there are few local minima, gradient-based algorithms can be conveniently restarted from many different (often randomly chosen) initial points and the best solution taken as the approximation of the global minimum. However, the number of additional minima grows rapidly as the number of equivalent-circuit elements is increased.

Alternatives to gradient-descent-based parameter extraction have recently been proposed by Vai *et al.* [1]–[3] who used simulated annealing (SA) [4] and Bilbro *et al.* [5] who used tree annealing (TA)—a modified form of simulated annealing. These are global optimization techniques. SA differs from descent algorithms by continually accepting some proportion of random moves up the error surface. SA is more efficient than random multistart descent algorithms if the local minima tend to be shallow and if the error

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